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August 22, 1997

BOX PATENT APPLICATION
Assistant Commissioner of Patents
Washington, D.C. 20231

Re: Reissue of U.S. Patent **5,444,305**
Reissue Application of Yoshinori MATSUI
SEMICONDUCTOR MEMORY CIRCUIT
Our Ref: Q46364

Dear Sir:

This is a request for filing a Reissue Application of U.S. Patent No 5,444,305 invented by Yoshinori Matsui. The patent issued on August 22, 1995 and is entitled SEMICONDUCTOR MEMORY CIRCUIT.

The following items are being submitted herewith:

1. An executed Reissue Declaration and Power of Attorney
2. Request for Title Report
3. Assent of Assignee to Reissue
4. Certificate under 37 C.F.R. § 3.73(b)
5. Offer to Surrender Letters Patent
6. A copy of U.S. Patent 5,444,305 with each column on a separate page and the requested claim changes for the reissue

The original Letter Patent will be submitted in due course.

Please transfer the drawings from prior Application No. 08/084,017, on which U.S. Patent 5,444,305 issued, as there are no changes to the drawings. Copies of the original drawings are enclosed herewith.

Priority is claimed from June 30, 1992, based on Japanese Application No. 4-172229. The priority document was filed in parent Application No. 08/084,017.

The Government filing fee is calculated as follows:

Independent Claims	6	-	3	=	3	x	$80.00	= $ 240.00
Total Claims	20	-	0	=	0	x	$22.00	= $ 0.00
Multiple Dependent Claim Fee ($260.00)								$ 0.00
Base Fee								$ 770.00
TOTAL FILING FEE								**$1,010.00**

A check for the filing fee of **$1,010.00** is attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Respectfully submitted,

By _____
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Date: August 22, 1997

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United States Patent [19]

Matsui

[11] Patent Number: 5,444,305

[45] Date of Patent: Aug. 22, 1995

[54] SEMICONDUCTOR MEMORY CIRCUIT

[75] Inventor: Yoshinori Matsui, Tokyo, Japan

[73] Assignee: NEC Corporation, Tokyo, Japan

[21] Appl. No.: 84,017

[22] Filed: Jun. 30, 1993

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Jun. 30, 1992 [JP] Japan 4-172229

[51] Int. Cl.[6] G11C 7/00

[52] U.S. Cl. 365/207; 365/189.01; 365/221; 365/230.03; 365/230.04

[58] Field of Search 365/189.01, 230.03, 365/221, 207, 230.04, 196

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SEMICONDUCTOR MEMORY CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a semiconductor memory circuit, and more particularly to a semiconductor memory circuit which includes shared sense amplifiers and is adapted for multibit parallel input and output configuration and for increasing the capacity.

2. Description of the Prior Art

In semiconductor memory circuits, the folded bit line structure in which a bit line for giving a reference potential to a sense amplifier (referred to as bit line for reference potential hereinafter) and a bit line for reading out data of a memory cell (referred to as bit line for read hereinafter) are arranged on one side of the sense amplifier, gives less induced noise to the bit line compared with the open bit line structure in which the bit line for reference potential and the bit line for read are arranged on the mutually opposite sides of the sense amplifier, so that it is currently in widespread use for semiconductor memory circuits.

Moreover, since in a semiconductor memory circuit such as a dynamic RAM (referred to as DRAM hereinafter) the ratio of the capacity of the memory cell capacitor (referred to as capacity of memory capacitor hereinafter) to the parasitic capacity of the bit line (referred to as capacity of bit line hereinafter) is related directly to the read voltage generated in the bit line, this ratio is an important parameter for the design of DRAM. The capacity of bit line is determined by the number, the size, and the structure of memory cells connected to the bit line, and the structure, size, material, or the like of the bit line itself. Accompanying the advancement of the generation of semiconductor memory circuits and the increase of the memory capacity, geometrical refinement of the memory cell and the bit line is advanced and the capacity of bit line is decreased. On the other hand, it brings about a decrease of the capacity of memory capacitor and an increase of the induced noise, and the number of the memory cells connected to one bit line has not been changed since it was increased from 64 bits to 128 bits for 256 kbit DRAM, even for the advances of the memory capacity of 1M bits, 4M bits, and 16M bits. Various kinds of split bit line modes have been proposed in order to keep the number of memory cells connected to one bit line constant, in the midst of the alternation of generation of DRAM as mentioned above, under the condition of limited chip size. Among them, the multisplit bit line shared sense amplifier mode (referred to as shared sense amplifier mode hereinafter) is being adopted most widely for the reasons that it is possible to realize a reduction of power consumption and an improvement of operating speed, and is most advantageous from the viewpoint of chip size (see for example, 16Mbit DRAM μPD4216400 made by NEC Corporation which is the assigned of this application).

Next, an example of semiconductor memory circuit of the shared sense amplifier mode will be described.

This semiconductor memory circuit comprises a plurality of memory cell arrays each including a plurality of memory cell trains connected respectively to bit line pairs of folded bit line mode, and are arranged in the direction in which each of these memory cell train extends while keeping the mutual correspondence relation among these memory cell trains, a plurality of first

selection/sense amplifier circuits each including first selection means which is arranged in every interarray regions between the pair of mutually adjacent memory cell arrays and selects for each member of the respective pairs either of an odd-numbered train or an even-numbered train of the plurality of memory cell trains of the memory cell arrays on both sides of the interarray region, a plurality of sense amplifiers which amplify the respective read data of the memory cell trains selected by the first selection means in one-to-one basis, and second selection means which selects one of the plurality of sense amplifiers and one of the memory cell trains selected by the first selection means and connect them to the corresponding data input and output lines, and transmits one of the amplified read data of an odd-numbered or an even-numbered memory cell train of the selected memory cell array on one side to the corresponding data input and output lines and supplies write data transmitted to the corresponding data input and output lines to a selected memory cell train of a selected memory cell array, two units of second selection/sense amplifier circuits each including a plurality of sense amplifiers arranged on the outside of the respective memory cell arrays at both ends of the disposition of the plurality of memory cell arrays and amplify in one-to-one basis read data of memory cell trains set differently from those of the first selection/sense amplifier circuits corresponding to the outermost memory cell arrays and selection means which selects one of the plurality of the sense amplifiers and one of the set memory cell trains of the outermost memory cell array and connects them to corresponding data input and output lines, and transmit amplified read data from the set memory cell trains of the outermost memory cell arrays to corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines to selected memory cell trains of the outermost memory cell arrays, a plurality of data buses corresponding to the respective bits of data which is transferred in bit parallel mode between an external circuit, and a plurality of input and output switching circuits which transmit the respective read data from the memory cell arrays one by one to the corresponding data buses via the first and the second selection/sense amplifier circuits by sequentially assigning equal number of memory cell arrays in the order of arrangement to the plurality of data buses, respectively, and supply write data transmitted to these data buses from the external circuit to respective selected memory cell trains of the corresponding memory cell arrays.

If it is assumed in this semiconductor memory circuit that, for example, the number of the memory cell arrays is eight, the number of the data buses is four, and the data transfer between the external circuit is carried out in four bit parallel mode, then seven first selection/sense amplifier circuits are arranged among eight memory cell arrays, a second selection/sense amplifier circuit is arranged on the outside of the each of the outermost memory cell array of the eight memory cell arrays, and a plurality of input and output switching circuits are arranged between the first and second selection/sense amplifier circuits and four data buses. Since two memory cell arrays each are made to correspond sequentially in the order of arrangement to the respective members of the four data buses, the first and the second memory cell arrays from the left correspond to the first data bus, the third and the fourth memory cell arrays

correspond to the second data bus, the fifth and the sixth memory cell arrays correspond to the third data bus, and the seventh and the eighth memory cell arrays correspond to the fourth data bus. Further, if the first and the second selection/sense amplifier circuits are designated from the left as the first, the second, . . . , and the ninth sense amplifiers, the data transmission between the first and the second memory cell arrays and the first data bus is executed via the first, second, and the third selection/sense amplifier circuits, the data transmission between the third and the fourth memory cell arrays and the second data bus is executed via the third, the fourth, and the fifth selection/sense amplifier circuits, and similarly, the data transmission between the fifth and the sixth memory cell arrays and the third data bus is executed via the fifth, the sixth, and the seventh selection/sense amplifier circuits, and the data transmission between the seventh and the eighth memory cell arrays and the fourth data bus is executed via the seventh, the eighth and the ninth selection/sense amplifier circuits.

As in the above, in this semiconductor memory circuit, the third, the fifth, and the seventh selection/sense amplifier circuits have to carry out the data transfer between the respective two data buses. For this reason, it becomes necessary to have two input and output switching circuits between these selection/sense amplifier circuits and the data buses, and the layout becomes complicated and the chip area needs be increased accordingly.

BRIEF SUMMARY OF THE INVENTION

OBJECT OF THE INVENTION

It is therefore the object of this invention to provide a semiconductor memory circuit which enables one to simplify the layout and reduce the chip area.

SUMMARY OF THE INVENTION

The semiconductor memory circuit according to this invention comprises a plurality of memory cell arrays each including a plurality of memory cell trains, arranged adjacent with each other in a predetermined direction, a plurality of first selection/sense amplifier circuits arranged in every region between mutually adjacent pair of memory cell arrays, which amplify read data from memory cell trains alternately designated in the order of arrangement out of odd-numbered and even-numbered trains on one selected side of memory cell arrays on both sides of the region between the cell arrays, transmit one of the data to corresponding data input and output lines and supply write data transmitted to the corresponding input and output lines to selected memory cell train of selected memory cell array, two units of second selection/sense amplifier circuits arranged on the outside of the respective memory cell arrays on both ends of the plurality of memory cell arrays, which amplify read data from predetermined one memory cell train of odd-numbered and even-numbered trains of the outermost memory cell arrays and transmit one of the data to the corresponding data input and output lines and supply write data transmitted to the corresponding input and output lines to a selected memory cell train of the outermost memory cell array, a plurality of data buses corresponding to the respective bits of data transferred in bit parallel mode between the external circuit, and a plurality of input and output switching circuits arranged and connected respectively in one-to-one correspondence to the first and the second

selection/sense amplifier circuits and connected to the plurality of the data buses so as to have equal number of memory cell trains that can carry out data transfer with the respective data buses, and carry out data transfer between these data buses and the first and the second selection/sense amplifier circuits in one-to-one correspondence mode.

In this semiconductor memory circuit, the input and output switching circuits are arranged in one-to-one correspondence to the first and the second selection/-sense amplifier circuits, so that it is possible to simplify the layout and to decrease the chip area in proportion to the reduction in the number of input and output switching circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram for an embodiment of the invention;

FIG. 2 is a circuit diagram for the memory call arrays and first selection/sense amplifier circuits which constitute a part of the embodiment;

FIG. 3 is a block diagram for a modification of the embodiment; and

FIG. 4 is a block diagram for another modification of the embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, the semiconductor memory circuit which is an embodiment of the invention shown in this figure comprises a plurality of memory cell arrays MCA1 to MCA8 each indluding a plurality of memory cell trains, arranged in the direction of extension of these memory cell trains while keeping the correspondence relation among these memory cell trains, a plurality of first selection/sense amplifier circuits SSA11 to SSA17, each circuit including, first selection means arranged in the region between the cell arrays, namely, between memory cell arrays MCA1 and MCA2, between MCA2 and MCA3, between MCA3 and MCA4, . . . , and between MCA7 and MCA8, respectively, and selects out of the memory cell trains of the memory cell arrays on both sides of every region between the cell arrays either an odd-numbered train or an even-numbered train designated alternately in the order of arrangement, one side at a time, a plurality of sense amplifiers which amplify read data of memory cell trains selected by the first selection means in one-to-one correspondence, and second selection means which selects one of the sense amplifiers and one of the memory cell trains selected by the first selection means and connects them to corresponding data input and output lines, and transmit one of amplified read data of an odd-numbered or an even-numbered memory cell train of memory cell array on one side (MCA1, for example) to the corresponding data input and output lines, and supply write data transmitted to the corresponding data input and output lines to a selected memory cell train of a selected memory cell array (MCA1, for example), second selection/sense amplifier circuits SSA21 and SSA22 which include a plurality of sense amplifiers, different from the selection/sense amplifier circuits

SSA11 and SSA17, arranged in cell end regions outside of the memory cell arrays MCA1 and MCA8 and respectively amplify in one-to-one correspondence the read data of memory cell arrays and selection means which selects one of these sense amplifiers and one of designated odd-numbered or even-numbered memory cell trains and connect them to corresponding data input and output lines, and transmit amplified read data from designated odd-numbered or even-numbered memory cell train of the memory cell arrays MCA1 and MCA8 to corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines to selected memory cell trains of memory cell arrays MCA1 and MCA8, a plurality of data buses DB11/DB12 to DB41/DB42 which correspond to data D_1 to D_4, respectively, that are transferred in bit parallel manner between an external circuit, a plurality of input and output switching circuits IOS1 to IOS9 which are arranged in one-to-one correspondence to the first and the second selection/sense amplifier circuits SSA11 to SSA17/SSA21 and SSA22 and carry out one-to-one transfer of read data and write data between each of the data buses DB11/DB12 to DB41/DB42 and one of the corresponding selection/-sense amplifier circuits by connecting the first input and output terminals to the data input and output lines of the corresponding selection/sense amplifier circuits and the second input and output terminals to one of the data buses DB11/DB12 to DB41/DB42 so as to have the number of memory cell trains capable of carrying out data transfer with the data buses is mutually equal, and data input and output circuits DIO1 to DIO4 which output read data transmitted to the data buses DB11/DB12 to DB41/DB42 to the external circuit in bit parallel manner and transmit write data from the external circuit to the data buses DB11/DB12 to DB41/DB42 in bit parallel manner.

Referring to FIG. 2 showing a part of the embodiment in terms of a specific circuit diagram, it can be seen that this embodiment has the folded bit line structure in which a bit line (BL12, for example) that gives a reference potential to the sense amplifier (SA11, for example) and a bit line for data read (BL11, for example) are arranged mutually parallel on one side of a sense amplifier (SA11).

An odd-numbered or an even-numbered memory cell train of the memory cell array is formed by memory cells (MCs) that are connected to a pair of bit lines for reference potential and for data read. For example, in the memory cell array MCA1, the memory cell train corresponding to the bit line pairs BL11/BL12 and BL15/BL16 forms an odd-numbered train, while the memory cell train corresponding to BL13/BL14 and BL17/BL18 forms an even-numbered train.

A first selection/sense amplifier circuit (SSA11, for example) has sense amplifiers (SA11, SA12, . . .) provided one each for the memory cell train corresponding to one (odd-numbered train in SSA11) of odd-numbered and even-numbered trains of memory cell arrays on its both sides (MCA1 and MCA2, for example), data transfer circuits (DT11 and DT12) of the first selection means which selects, one side at a time, an odd-numbered or an even-numbered memory cell train of the memory cell arrays (MCA1 and MCA2) on both sides in response to transfer control signals (TG_{11} and TG_{12}) and connects it to the corresponding sense amplifier circuit, and a train selection circuit (YS1) of the second selection means which connects one of odd-numbered

or even-numbered memory cell train of the memory cell array selected by the data transfer circuits (DT11 and DT12) and one of the sense amplifier circuits selected in response to train selection signals (Y_{11}, Y_{12},) to data input and output lines (IO11 and IO12).

Further, since the second selection/sense amplifier circuits SSA21 and SSA22 merely make access to only one of odd-numbered and even-numbered trains of the memory cell trains of the memory cell arrays MCA1 and MCA2, each of them has one data transfer circuit (not shown in FIG. 2). The remaining construction is identical to the first selection/sense amplifier circuit. The access memory cell trains of the second selection/-sense amplifier circuits SSA21 and SSA22 are even-numbered trains since the access memory cell trains of the adjacent first selection/sense amplifier circuits SSA11 and SSA17 are odd-numbered trains.

As described in the above, the access memory cell trains of the first and the second selection/sense amplifier circuits SSA11 to SSA17/SSA21 and SSA22 are so fixed as to be alternately an odd-numbered and an even-numbered train according to the order of their arrangement, there is obtained a semiconductor memory circuit of the shared sense amplifier mode.

In this embodiment, the memory cell trains that can transfer data between the data buses DB11/DB12 via the selection/sense amplifier circuits SSA11 to SSA17/-SSA21 and SSA22 and the input and output switching circuits IOS1 to IOS9 are both the odd-numbered and even-numbered trains of the memory cell array MCA1, odd-numbered trains of the memory cell array MCA2, and even-numbered trains of the memory cell array MCA8, and the memory cell trains that can transfer data between the data buses DB21/DB22 are even-numbered trains of the memory cell array MCA2, both the odd-numbered and even-numbered trains of the memory cell array MCA3, and odd-numbered trains of the memory cell array MCA4. Similarly, for the data buses DB31/DB32, they are even-numbered trains of MCA4, both the odd-numbered and even-numbered trains of MCA5, and odd-numbered trains of MCA6, and for the data buses DB41/DB42, they are even-numbered trains of MCA6, both the odd-numbered and even-numbered trains of MCA7, and odd-numbered trains of MCA8. One each of the memory cell trains that can carry out data transfer between each of the data buses DB11/DB12 to DB41/DB42 is selected by the selection/sense amplifier circuits SSA11 to SSA17/-SSA21 and SSA22, and read for an external circuit of four-bit data D_1 to D_4 and write from the external circuit is carried out in bit parallel via the data input and output circuits DIO1 to DIO4.

In the conventional semiconductor memory circuit, the memory cell arrays that can transfer data between the data bus DB11/DB12 are MCA1 and MCA2, and similarly, for the data bus DB21/DB22 they are MCA3 and MCA4, for the data bus DB31/DB32 they are MCA5 and MCA6, and for the data bus DB41/DB42 they are MCA7 and MCA8. Accordingly, the selection/sense amplifier circuit SSA12 situated between the memory cell arrays MCA2 and MCA3 needs to perform data transfer with the two data buses DB11/DB12 and DB21/DB22, the selection/sense amplifier circuit SSA14 between the memory call arrays MCA4 and MCA5 needs to perform data transfer with the two data buses DB21/DB22 and DB31/DB32, and the selection/sense amplifier circuit SSA16 between the memory cell arrays MCA6 and MCA7 needs to perform data

transfer with the two data buses DB31/DB32 and DB41/DB42. Therefore, input and output circuits of two each are required between the selection/sense amplifier circuit SSA12, SSA14, SSA16 and the data buses DB11/DB12 to DB41/DB42, and it results in complication of the layout and increase of the chip area in proportion to this situation.

In contrast, in this invention one data bus is assigned to each of the selection/sense amplifier circuits SSA11 to SSA17/SSA21 and SSA22, so that the input and output switching circuit between each of these selection/sense amplifier circuits SSA11 to SSA17/SSA21 and SSA22 and the data buses DB11/DB12 to DB41/DB42 becomes one for each, and accordingly it is possible to simplify the layout and reduce the chip area.

Referring to FIG. 3 showing a modification of the embodiment, even-numbered trains (or odd-numbered trains) of the memory cell trains are made to correspond to odd-numbered data buses. The correspondence relation between the even-numbered train/odd-numbered train and the data buses can be anything provided that the number of the memory cell trains connectable to each data bus is equal.

Furthermore, the second selection/sense amplifier circuits SSA21 and SSA22 have memory cell trains of one of odd-numbered and even-numbered trains of the outermostly arranged memory cell arrays (MCA1 and MCA8) as the objects of access. Therefore, if the number of memory cell arrays connectable to one data bus is taken as the memory cell array unit (namely, the memory cell trains for an integral number of memory cell arrays), the second selection/sense amplifier circuits are connected without fail to the identical data bus via the corresponding input and output switching circuits. Accordingly, if the number of memory cells trains connectable to one data bus is set to be equal to an even number of times of the memory cell arrays, then the input and output switching circuit arranged at the center can also be made to be surely connected to the identical data bus for the outermost input and output switching circuits. Consequently, the pattern of the connection lines between the input and output switching circuits and the data buses can be made laterally symmetric with respect to the input and output switching circuit at the center, and the array design can further be facilitated. An example of the laterally symmetric pattern of the connection lines is shown in FIG. 4. There can be thought several patterns of laterally symmetric connection lines other than the one shown in FIG. 4, but a simple pattern with maximum regularity is advantageous.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that appended claims will cover any modifications or embodiments as fall within the true scope of the invention.

What is claimed is:

1. A semiconductor memory circuit comprising:

a plurality of memory cell arrays each consisting of a plurality of memory cell trains arranged in a direction in which these memory cell trains extend while keeping the mutual corresponding relationship among the memory cell trains;

a plurality of first selection/sense amplifier circuits including first selection means arranged in the respective regions between mutually adjacent pairs of said memory cell arrays for selecting one side at a time one of odd-numbered or even-numbered memory cell train out of the plurality of memory cell trains of the memory cell arrays on both sides of the regions between arrays, a plurality of amplifier means for amplifying in one-to-one correspondence the respective read data of memory cell trains selected by the first selection means, and second selection means for selecting one of the plurality of amplifier means and one of the memory cell trains selected by said first selection means and connecting them to corresponding data input and output lines, and transmit one of the amplified read data from a designated odd-numbered or even-numbered memory cell train of memory cell arrays on the selected one side to the corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines to selected memory cell trains of selected memory cell arrays; two units of second selection/-sense amplifier circuits including a plurality of amplifier means arranged on the outside of the memory cell arrays on both ends of the arrangement of said plurality of memory cell arrays for amplifying in one-to-one correspondence the respective read data of odd-numbered or even-numbered memory cell trains of said memory cell arrays on both ends defined differently from the first selection/sense amplifier circuits corresponding to said memory cell arrays on both ends and connection means for selecting one of the plurality of the amplifier means and one of the designated odd-numbered or even-numbered memory cell array of said memory cell arrays on both ends and connecting them to corresponding data input and output lines, which transmit one of the amplified read data from the designated odd-numbered or even-numbered memory cell trains of the memory cell arrays on said both ends to said corresponding data input and output lines and supply write data transmitted to the corresponding data input and output lines from the external circuit to selected memory cell trains of said memory cell arrays on both ends; a plurality of data buses corresponding to each of the respective bits of data transferred in bit parallel mode between the external circuit; and a plurality of input and output switching circuits arranged in one-to-one correspondence to said plurality of first and second selection/sense amplifier circuits with their first input and output terminals connected to the data input and output lines of the corresponding selection/sense amplifier circuits and their second input and output terminals connected to one of said plurality of data buses so as to make the number of memory cell trains which makes the data transfer to the respective data buses, to carry out data transfer between each of said data buses and one of the corresponding selection/sense amplifier circuit;

wherein the number of memory cell trains capable of transferring data to the respective members of said plurality of data buses is set to be an even multiple of the number of said memory cell arrays, the second input and output terminals of the input and output switching circuits corresponding to said

second selection/sense amplifier circuits and the input and output switching circuit corresponding to the first selection/sense amplifier circuit arranged at the center of the first selection/sense amplifier circuits are connected to an identical data bus of the plurality of said data buses, and the second input and output terminals of the input and output switching circuits other than these input and output switching circuits are connected to the corresponding data buses so as to be laterally symmetric with respect to the connection line to the data bus of the input and output switching circuit corresponding to said first selection/sense amplifier circuit arranged at the center as the center line of symmetry.

2. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second group of memory cells, said memory cell blocks being arranged in a first direction;

a first amplifier block provided adjacently to one end of an arrangement of said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on said one end, and selectively transferring a data of one of said memory cells in said one of said first and second groups via a first internal data line extending in a second direction different from said first direction;

a second amplifier block provided adjacently to another end of said arrangement, coupled to one of said first and second groups in one of said memory cell blocks on said another end, and selectively transferring a data of one of said memory cells in said one of first and second groups via a second internal data line thereof extending in said second direction;

at least one third amplifier block arranged between said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks adjacent to one side thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to another side thereof, and selectively transferring a data of one of said groups

coupled thereto via a third internal data line thereof extending along said second direction;

a first data line extending along said first direction and coupled commonly to said first and second internal data lines in said first and second amplifier blocks while being isolated from said third internal data line in said third amplifier block, said first and second amplifier blocks thereby being coupled to a common first input-output circuit via said first data line independently from said third amplifier block;

a second data line extending along said first direction and coupled to said third internal data lines in said third amplifier block and thereby coupling said third amplifier block to a second input-output circuit independently from said first and second amplifier blocks.

3. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second memory cell;

a plurality of amplifier blocks, said memory cell blocks and said amplifier blocks being arranged alternately to form an array extending along a first direction, said array having on both ends thereof said amplifier blocks, thereby each of said memory cell blocks having both sides thereof on said first direction facing to said amplifier blocks, each of said memory cell blocks having said first and second memory cells thereof coupled to said amplifier blocks on one and another sides thereof, respectively;

a first data line for selectively connecting said amplifier blocks on said both ends of said array commonly to a first input-output circuit, thereby said first input-output circuit being associated with a first number of said first and second memory cells for read or write operation of said memory device;

a second data line for selectively connecting at least one of said amplifier blocks other than said amplifier blocks coupled to said first input-output circuit to a second input-output circuit, thereby said second input-output circuit being associate with said first number of said first and second memory cells for said operation of said memory device.

* * * * *

4. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second group of memory cells, said memory cell blocks being arranged in a first direction;

a first amplifier block provided adjacently to one end of an arrangement of said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks on said one end, and selectively transferring a data of one of said memory cells in said one of said first and second groups via a first internal data line extending in a second direction different from said first direction;

a second amplifier block provided adjacently to another end of said arrangement, coupled to one of said first and second groups in one of said memory cell blocks on said another end, and selectively transferring a data of one of said memory cells in said one of first and second groups via a second internal data line thereof extending in said second direction;

at least one third amplifier block arranged between said memory cell blocks, coupled to one of said first and second groups in one of said memory cell blocks adjacent to one side thereof, and to one of said first and second groups in one of said memory cell blocks adjacent to another side thereof, and selectively transferring a data of one of said groups coupled thereto via a third internal data line thereof extending along said second direction;

a first data line extending along said first direction and coupled commonly to said first and second internal data lines in said first and second amplifier blocks while being isolated from said third internal data line in said third amplifier block; and

a second data line extending along said first direction and coupled to said third internal data lines in said third amplifier block.

5. A semiconductor memory device as claimed in claim 4, further comprising a first interface circuit coupled to said first data line and a second interface circuit coupled to said second data line, said first and second amplifier blocks thereby being coupled to said first interface circuit in common via said first data line independently from said third amplifier block,

and said third amplifier block thereby being coupled to said second interface circuit independently from said first and second amplifier blocks.

6. A semiconductor memory device as claimed in claim 5, wherein:

said first interface circuit operatively receives read data from one of said first and second amplifier blocks; and

said second interface circuit operatively receives read data from said third amplifier block.

7. A semiconductor memory device as claimed in claim 6, wherein said first and second interface circuits operatively transfer write data to be written in said memory device.

8. A semiconductor memory device as claimed in claim 4, wherein:

each of said memory cell blocks has the memory cells thereof arranged in rows and numbered columns to form a matrix, said columns including even and odd numbered columns;

each of said columns extends in said first direction;

for each of said memory cell blocks, said even numbered columns comprise one of said first and second groups of memory cells, and said odd numbered columns include the other of said first and second groups of memory cells.

9. A semiconductor memory device as claimed in claim 8, further comprising:

a plurality of sense amplifiers in each of said first, second and third amplifier blocks, each of said sense amplifiers having a pair of input nodes; and

a plurality of pairs of parallel bit lines extending in said columns, one and another of bit lines in one of said pairs of bit lines providing a reference potential and a read signal to be applied to said sense amplifier, said sense amplifier in said third amplifier block having said pair of input nodes thereof operatively connected to either one of said pairs of bit lines in one of said memory cell block facing to one side of said third amplifier block and another pair of bit lines in another memory cell block facing to another side of said third amplifier block.

10. A semiconductor memory device as claimed in claim 9, further comprising:

a plurality of first pairs of transfer gate transistors each arranged between one of said pairs of bit lines and associated one of said sense amplifiers operatively providing a current path between one of said bit lines in said pair of bit lines and one of said nodes of said sense amplifier and simultaneously providing another current path between another of said bit lines in said pair of bit lines and another of said nodes of said sense amplifier in response to a transfer control signal.

11. A semiconductor memory device as claimed in claim 10, further comprising a plurality of second pairs of transfer gate transistors each associated with one of said sense amplifiers in said first, said second and said third amplifier blocks, each of said pairs of second transfer gate transistors selectively providing a first current path between one of said nodes of said sense amplifier and one of said first, said second and said third internal data line and a second current path between another of said nodes of said sense amplifier and a complement data line associated with said one of said first, said second and said third internal data lines.

12. A semiconductor memory device comprising:

a plurality of memory cell blocks each including a first and a second memory cell;

a plurality of amplifier blocks, said memory cell blocks and said amplifier blocks being arranged alternately to form an array extending along a first direction, said array having on both ends thereof said amplifier blocks, thereby each of said memory cell blocks having both sides thereof on said first direction facing to said amplifier blocks, each of said memory cell blocks having said first and second memory cells thereof coupled to said amplifier blocks on one and another sides thereof, respectively;

a first data line coupled to said amplifier blocks on said both ends of said array commonly and associated with a number of said first and second memory cells for read or write operation of said memory device; and

a second data line coupled to at least one of said amplifier blocks other than said amplifier blocks coupled to said first data line, said second data line being isolated from said first data line and associated with said number of said first and second memory cells for said operation of said memory device.

13. A semiconductor memory device as claimed in claim 12, further comprising a first data transfer circuit coupled to said first data line and selectively coupled to said amplifier blocks on said both ends of said array via said first data line, said first data transfer circuit being associated with said number of memory cells, and a second data transfer circuit coupled to said second data line and selectively coupled to said at least one amplifier block via said second data line, said second data transfer circuit being associated with said number of memory cells.

14. A semiconductor memory device as claimed in claim 13, wherein said first and second data transfer circuits receive read data of the memory device via said first and second data lines.

15. A semiconductor memory device as claimed in claim 12, wherein each of said memory cell blocks includes said memory cells arranged in rows and columns, said columns extending in said first direction, one of said first and second memory cell belonging to an even numbered column, another of said first and second memory cell belonging to an odd numbered column.

16. A semiconductor memory device as claimed in claim 15, further comprising:

a sense amplifier in each of said amplifier blocks, said sense amplifier having a pair of input nodes; and

a pair of bit lines in each of said columns, said pair of bit lines being arranged in a folded bit line structure having one and another of said bit lines in said pair of bit lines providing a reference potential and a read signal to be applied to said sense amplifier, said sense amplifier in one of said amplifier blocks arranged between two of said memory cell blocks having said pair of input nodes thereof operatively connected to one pair of bit lines in one column in either one of said two memory cell blocks.

17. A semiconductor memory device as claimed in claim 16, further comprising:

a first pair of transfer gate transistors selectively providing current paths between said pair of input nodes of said sense amplifier in one of said amplifier blocks arranged between two

of said memory cell blocks and one pair of bit lines in one column in either one of said two memory cell blocks in response to a first transfer control signal; and a second pair of transfer gate transistors selectively providing current paths between said pair of input nodes of said sense amplifier and another pair of bit lines in another column in another of said two memory cell blocks in response to a second transfer control signal.

18. A semiconductor memory device as claimed in claim 17, further comprising:

a pair of signal lines extending in each of said amplifier blocks and in a second direction perpendicular to said first direction; and

a selection circuit in each of said amplifier blocks providing current paths between said input nodes of selected one of said amplifiers and said pair of signal lines according to a selection signal, said pair of signal lines being coupled to one of said data lines via a switching circuit.

19. A combination of amplifier blocks and memory cell blocks comprising:

N amplifier blocks arranged in a first direction, said N amplifier blocks including a first amplifier block, a last amplifier block, and a remainder of amplifier blocks;

N-1 memory cell blocks, each arranged between and coupled with two respectively adjacent ones of said N amplifier blocks, said remainder of amplifier blocks each being shared by two respectively adjacent ones of said memory cell blocks;

a first data line coupled to said first amplifier block and said last amplifier block; and

a second data line coupled to one of said remainder of amplifier blocks, said second data line being isolated from said first amplifier block and said last amplifier block.

20. A combination as claimed in claim 19, further comprising:

for each of said amplifier blocks, a respective signal line, extending in a second direction perpendicular to said first direction, for transferring a data signal from an associated one of said memory cell blocks;

said first data line being coupled, at a first side thereof, to said respective signal line of said first amplifier block;

said first data line being coupled, at a second side thereof, to said respective signal line of said amplifier block.

[57] ABSTRACT

This semiconductor circuit includes a plurality of memory cell arrays arranged mutually adjacent in one direction, a plurality of first selection/sense amplifier circuits provided in the respective regions between mutually adjacent pairs of these memory cell arrays and make access to one of alternately defined odd-numbered or even-numbered memory cell trains in the order of arrangement, two units of second selection/sense amplifier circuits arranged on the outside of the memory cell arrays on both ends of the arrangement of the plurality of memory cell arrays and make access to one of the designated odd-numbered or even-numbered memory cell trains of the memory cell arrays on both ends, a plurality of data buses corresponding to the respective bits of data transferred in bit parallel between an external circuit, and a plurality of input and output switching circuits arranged and connected in one-to-one correspondence to the respective first and second selection/-sense amplifier circuits connected to the plurality of data buses so as to have an equal number of memory cell trains capable of transferring data with these data buses, and a plurality of input and output switching circuits which transfer data with the first and the second selection/sense amplifier circuits in one-to-one correspondence.

3 Claims, 4 Drawing Sheets

PATENT APPLICATION
Q46364

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yoshinori MATSUI

Reissue Application of U.S. Patent
No. 5,444,305 issued on August 22, 1995

Filed: Herewith

For: SEMICONDUCTOR MEMORY CIRCUIT

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175

I, Yoshinori Matsui, of Tokyo, Japan, do hereby declare and state as follows:

My residence, post office address, and citizenship are as stated below next to my name.

I believe that I am the original, first, and sole inventor of the invention "SEMICONDUCTOR MEMORY CIRCUIT" which is described and claimed in the above-identified U.S. Patent No. 5,444,305, issued August 22, 1995 and assigned to NEC Corporation, the specification of which is submitted with this application for reissue; and that I have reviewed and understand the contents of the specification, including the claims, as amended in this application for reissue.

In compliance with 37 C.F.R. § 1.175(a)(7), I hereby acknowledge my duty to disclose information of which I am aware which is material to the examination of this application for reissue.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119 or 365 from the following foreign application for patent: Japanese Patent Application No. 4-172229, filed in Japan on June 30, 1992. The priority document was filed in U.S. patent application 08/084,017.

Further, in compliance with 37 C.F.R. §§ 1.175(a)(1)-(a)(3), I hereby declare and state that the above-identified U.S. Patent No. 5,444,305 is believed to be at least partly inoperative for the reason that I claimed less than I had the right to claim in the patent.

The purpose of seeking a reissue patent is to address the insufficiency in the patented claims by presenting new claims which are commensurate with the true scope of my invention.

Pursuant to 37 C.F.R. § 1.175(a)(5)-(6), I below describe the particular errors in the patent, how these errors occurred, and I hereby aver that such errors arose without any deceptive intention.

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175
REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

A. Errors in the patent

The specific errors in the patent, i.e., every difference between the original patent and the claims sought to be added by this reissue application, are identified below.

The subject matter encompassed by original patent claims 1-3 is literally too narrow in certain respects to afford patent coverage commensurate with the true scope of my invention. As well, the patent lacks any dependent claims and fails to comprehensively claim the invention.

In general, claim 1 recites entirely too many specific limitations even to approximate the proper scope of my invention which resides not merely in the arrangement of the myriad particular circuits but more correctly in the overall arrangement of the memory cell blocks and the amplifier blocks. Claim 2 includes an unnecessary limitation in that it recites input-output circuits not necessary for patentability. Claim 3, like claim 2, also recites input-output circuits which are unnecessary for patentability.

New claims 4-20 presented in this reissue application include independent claims 4, 12, and 19. These new independent claims do not include all of the specific structure of issued claim 1, and are free of the input-output circuits of issued claims 2 and 3. Such limitations which are unnecessary for patentability are included in the claims which depend from new independent claims 4, 12, and 19. Therefore, these new claims more properly claim the true scope of my invention, and thus remedy the basic error in claiming less than I had a right to claim.

More particularly, new independent claim 4 provides a claim in the patent which does not have the above-identified error of claim 2; new independent claim 12 provides in the patent a claim which corrects the error of claim 3 being too narrow; and new independent claim 19 provides in the patent a claim that is even broader in some respects than new independent claims 4 and 12, thus claiming the invention with the scope to which it is entitled.

The specific differences between new claims 4-20 and the original patent claims, and the reasons for these differences, are explained below.

Claims 4-12

New independent claim 4 corrects an error in issued claim 2. Claim 2 has an error in that it has too narrow of a scope. In addition, claim 2 has an error in that it lacks the dependent claims necessary so as comprehensively to claim the subject matter of the invention.

Claim 2 has a scope that is too narrow because it includes limitations unnecessary to patentability, to wit, first and second input-output circuits. The first and second input-output circuits are believed to be unnecessary to the patentability of the claim because the subject matter of the claim could have been patentably distinguished with reference only to its simplified layout of a memory circuit with a particular arrangement of memory cell blocks, amplifier blocks, and data lines. I now explain how new claim 4 corrects this error.

New independent claim 4 recites exactly the same semiconductor memory device as set forth in issued claim 2 with two exceptions. The first exception is that claim 4 does not include the following requirement (which is included in lines 20-22 of claim 2, as shown in the Reissue Application which is being filed concurrently herewith): ", said first and second amplifier blocks thereby being coupled to a common first input-output circuit via said first data line independently from said third amplifier block". The second exception is that claim 4 does not include the following requirement (which is included in lines 24-25 of claim 2): "and thereby coupling said third amplifier block to a second input-output circuit independently from said first and second amplifier blocks".

Since new claim 4 omits the first and second input-output circuits, which are not necessary for patentability, claim 4 corrects the above-identified error of issued claim 2.

New dependent claims 5-11 correct the other error of claim 2, namely, that claim 2 as issued lacks the dependent claims necessary to comprehensively claim the invention. New dependent claims 5-11 add requirements to the subject matter of claim 4 as described now with particularity.

New dependent claim 5 (i.e., 5/4) contains limitations substantially similar to those which were omitted from claim 4 but included in issued claim 2. The limitations contained in claim 5, however, are not identical to those which were omitted from claim 4 but included in issued claim 2. In particular, claim 5 requires first and second interface circuits instead of "input-output" circuits as required in issued claim 2. I respectfully submit that the recitation of interface circuits encompasses more kinds of circuits than the narrower recitation of input-output circuits.

New claim 6 (i.e., 6/5/4) adds limitations not included in issued claim 2, to wit, the requirement for the first and second interface circuits to receive read data from the memory cell blocks.

New claim 7 (i.e., 7/6/5/4) also adds limitations not included in issued claim 2. Claim 7 requires that the first and second interface circuits transfer write data for the memory device.

New claim 8 (i.e., 8/4) adds limitations not included in issued claim 2. In particular, claim 8 requires that the memory cells of the memory cell blocks be arranged in rows and columns to form a matrix. Moreover, claim 8 adds the new requirement that the first group of memory cells be in either an even or an odd numbered column, and that the second group be in the other (i.e., if the first group is even, the second group is odd).

New claim 9 (i.e., 9/8/4) adds further limitations not included in issued claim 2. To be precise, claim 9 substantially describes a folded bit line structure. Also, new claim 9 describes how the third amplifier block is connected to the bit lines of its adjacent memory cell blocks.

New claim 10 (i.e., 10/9/8/4) adds limitations relating to first transfer gates, which were not mentioned in issued claim 2.

New claim 11 (i.e., 11/10/9/8/4) requires second transfer gates, another requirement not included in issued claim 2.

Claims 12-18

New independent claim 12 corrects an error in issued claim 3. Claim 3 has an error in that it has too narrow of a scope. Claim 3 has an additional error in that it lacks the dependent claims necessary so as comprehensively to claim the full extent of the invention.

Like issued claim 2, claim 3 has a scope that is too narrow because it includes limitations unnecessary to patentability, to wit, first and second input-output circuits. The first and second input-output circuits are believed to be unnecessary to the patentability of the claim because the subject matter of claim 3 could have been patentably distinguished with reference only to its simplified layout of a memory circuit with a particular arrangement of memory cell blocks, amplifier blocks, and data lines. I now explain how new claim 12 corrects this error.

New independent claim 12 is very similar to claim 3 in a substantive manner, but differs in that the claim omits any mention of the input-output circuits. Since new claim 12 omits the first and second input-output circuits, which are not necessary for patentability, claim 12 corrects the above-identified error of issued claim 3.

New dependent claims 13-18 correct the above-identified additional error of issued claim 3. That is, new dependent claims 13-18 (each of which depends directly or indirectly from new independent claim 12) provide the additional limitations necessary for the comprehensive claiming of the full extent of the invention.

In particular, new claim 13 (i.e., 13/12) requires data transfer circuits. The requirement for input-output circuits was omitted from independent claim 12 to correct an error in issued claim 3 and was moved to this dependent claim. Instead of reciting "input-output circuits", however, new claim 13 requires data transfer circuits.

New claim 14 (i.e., 14/13/12) adds a limitation not included in issued claim 3. That is, new claim 14 requires that the data transfer circuits handle read data of the memory device via first and second data lines.

New claim 15 (i.e., 15/12) includes the requirement that the memory cells be arranged in rows and columns with particular limitations relating to even and odd numbered columns. These requirements were not included in issued claim 3.

New claim 16 (i.e., 16/15/12) adds the requirement for a folded bit line structure and particular limitations relating to the coupling between amplifier blocks and their adjacent memory cell blocks. These requirements were not included in issued claim 3.

New claim 17 (i.e., 17/16/15/12) adds limitations not included in issued claim 3. In particular, claim 17 requires first and second transfer gate transistors which were not mentioned in claim 3.

New claim 18 (i.e., 18/17/16/15/12) adds the requirement for a switching circuit responsive to a selection signal; this requirement was not included in issued claim 3.

Claims 19 and 20

The patent is inoperative in that issued claims fail to recite the scope to which the invention is entitled. New independent claim 19 is even broader, in some respects, than any of independent claims 1, 2, 3, 4, and 12. By adding new independent claim 19, I achieve patent protection of a scope having the breadth to which the invention is entitled.

New claim 19 requires "first to N-th" amplifier blocks, instead of the plurality of amplifier blocks mentioned in claims 2, 3, 4, and 12, and instead of the plurality of

selection/sense amplifier circuits mentioned in claim 1. Similarly, new claim 19 requires "first to (N-1)-th memory cell blocks", instead of the plurality of memory cell blocks required in claims 2, 3, 4, and 12, and instead of the plurality of memory cell arrays required in claim 1.

In new claim 19, the first data line is "coupled" to "said first amplifier block and said N-th amplifier block", whereas in the other claims the first data line is coupled to the amplifier blocks on the ends of the array and also is isolated from another component. New claim 19 does not require the isolation of the first data line.

Claim 19 is thus not as narrow as the other independent claims in that it does not require the isolation of the first data line. Claim 19 is believed to more correctly claim the full breadth of patent protection to which my invention is entitled.

New dependent claim 20 (i.e., 20/19) adds to the invention as claimed in claim 19 the requirements for a signal line in each amplifier block, and describes a particular coupling for the signal lines for the first and for the (N-1)-th amplifier blocks.

B. How the above errors arose or occurred

Having discussed above the particular errors in the patent for which correction by reissue is sought, and having pointed out every difference between the original claim and reissue claim pursuant to 37 C.F.R. § 1.175(a)(3), I now explain how the errors arose or occurred, as required by 37 C.F.R. § 1.175(a)(5).

The errors arose during preparation and prosecution of U.S. Application No. 08/084,017 (the '017 application) which issued as U.S. Patent No. 5,444,305 (the '305 patent). Through oversight, I failed initially to have included claims having the scope of new claims 4-20, which are of varying scope and which are broader in at least some respects and narrower in other respects than original patent claims 1-3.

Through the Intellectual Property Division (IPD) of my company, NEC Corporation, I provided a substantially complete draft application to my U.S. attorneys (the Sughrue law firm), shortly before the expiration of the one year period for claiming foreign priority from my Japanese parent application and, after review, my U.S. attorneys filed the application in the U.S. Patent and Trademark Office.

In preparing the draft patent application, IPD failed to include claims having scopes such as that of the new claims proposed herewith.

The error of not including claims such as new claims 4-20 was not discovered during prosecution of the '017 application. In particular, the Examiner allowed dependent application claim 3 in the first Office Action. The IPD drafted an Amendment in which this claim was placed in independent form (this amended claim issued as claim 1). Two new claims 4 and 5 (which issued as claims 2 and 3, respectively) were added as well. These two new claims were directed to the invention in a different scope, but still were insufficient with respect to what I had a right to claim. This draft Amendment was sent to my U.S. attorneys shortly before the time limit for responding to the Office Action. The U.S. attorneys also failed to appreciate the full breadth of that to which I had a right to claim.

In the second Office Action, application claims 3 and 4 were rejected under only 35 U.S.C. § 112, second paragraph. IPD handled the rejection without a particular review of the scope of each claim. The '305 patent was thus passed to issue.

My company recently has reviewed the '305 patent in connection with the ordinary course of its business. During this review, the IPD asked me to review the '305 patent. I indicated to my company the importance of the '305 patent from a technical standpoint, and the IPD and I reviewed the claims to detect any possible insufficiency.

This review revealed that an error exists in the claims because they are not directed to the full scope of the invention (as already explained above, in detail).

New claims 4-20 are therefore being added by this reissue application in order to correct a deficiency in the patent, *viz.*, that through an oversight I failed to include claims having a scope commensurate with my true invention. New claims 4-20 particularly point out and distinctly claim my invention, and are believed to be patentable over the prior art.

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I.

REISSUE DECLARATION UNDER 37 C.F.R. § 1.175
REISSUE APPLICATION OF U.S. PATENT NO. 5,444,305

Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484, Mark Boland, Reg. No. 32,197, William H. Mandir, Reg. No. 32,156, Scott M. Daniels, Reg. No. 32,562, Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276; Bruce E. Kramer, Reg. No. 33,725; Paul F. Neils, Reg. No. 33,102; and Brett S. Sylvester, Reg. No. 32,765, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to **SUGHRUE, MION, ZINN, MACPEAK & SEAS**, PLLC, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: August 18, 1997

Inventor: Yoshinori Matsui
First Name Last Name

Residence: Japan

Signature: Yoshinori Matsui

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7-1, Shiga 5-chome, Minato-ku
Tokyo 108-01, JAPAN

Citizenship: Japan

PATENT APPLICATION
Q46364

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Yoshinori MATSUI

Reissue Application of U.S. Patent
No. 5,444,305 issued on August 22, 1995

Filed: Herewith

For: SEMICONDUCTOR MEMORY CIRCUIT

ASSENT OF ASSIGNEE TO REISSUE

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

NEC Corporation, the Assignee of the entire right, title, and interest of the invention described and claimed in the above-identified U.S. Patent No. 5,444,305, hereby assents to the reissue of said patent in accordance with the Reissue Declaration and accompanying papers submitted herewith.

NEC Corporation

Date: August 19, 1997

Signature

Shigemichi Nidaira
Typed or printed name

Vice President
Intellectual property
Title

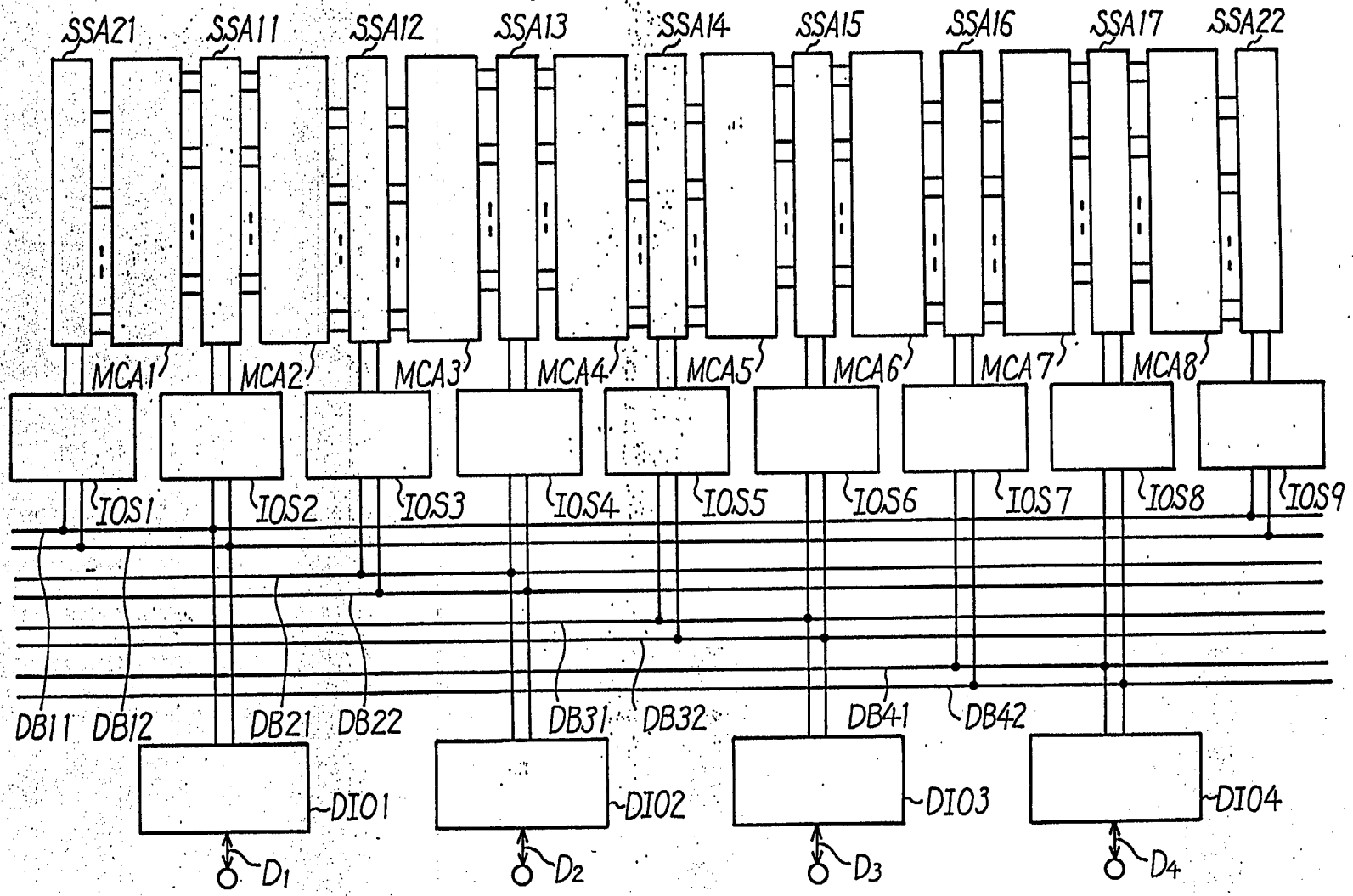
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FIG. 1

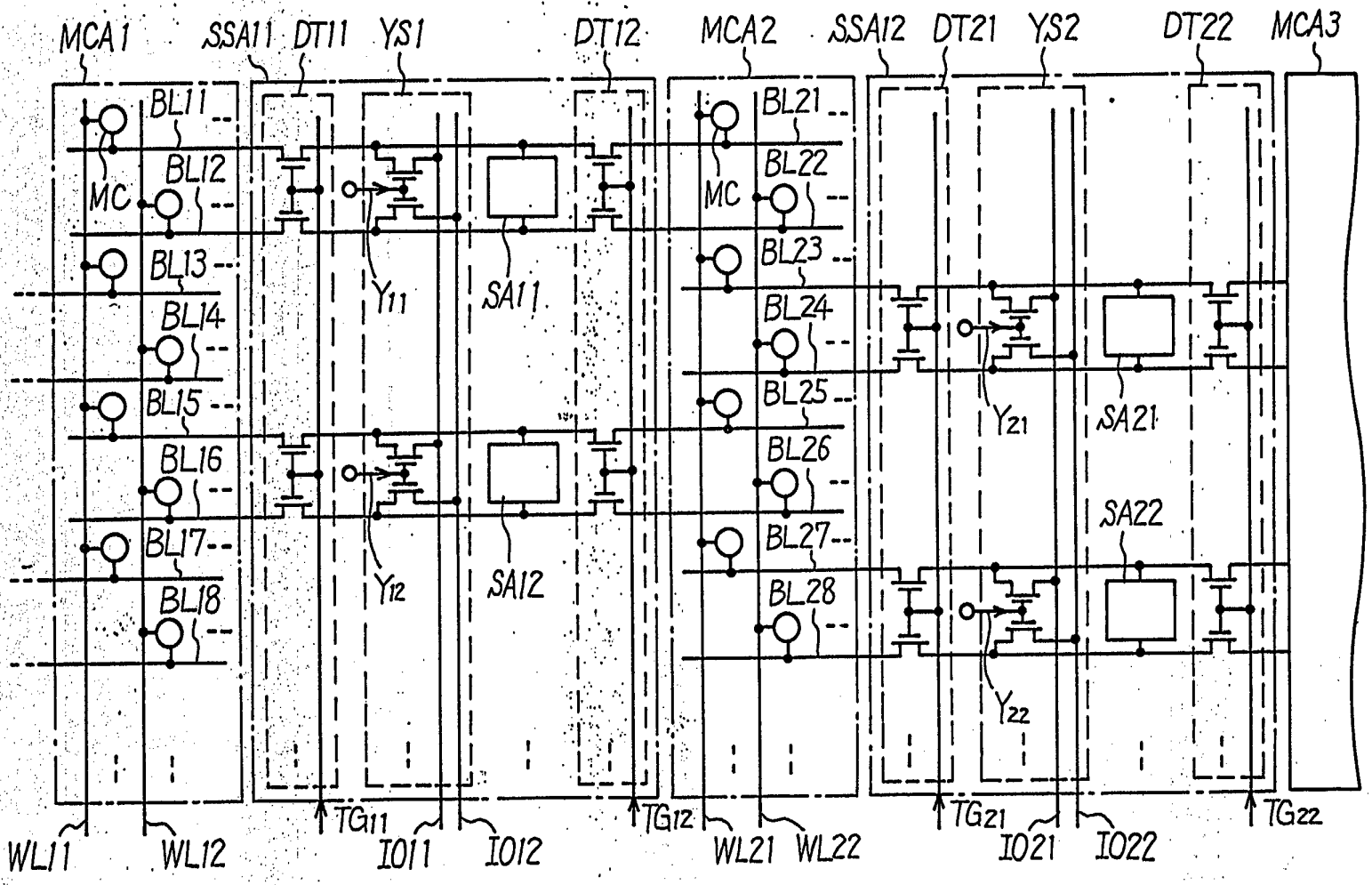
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FIG. 2

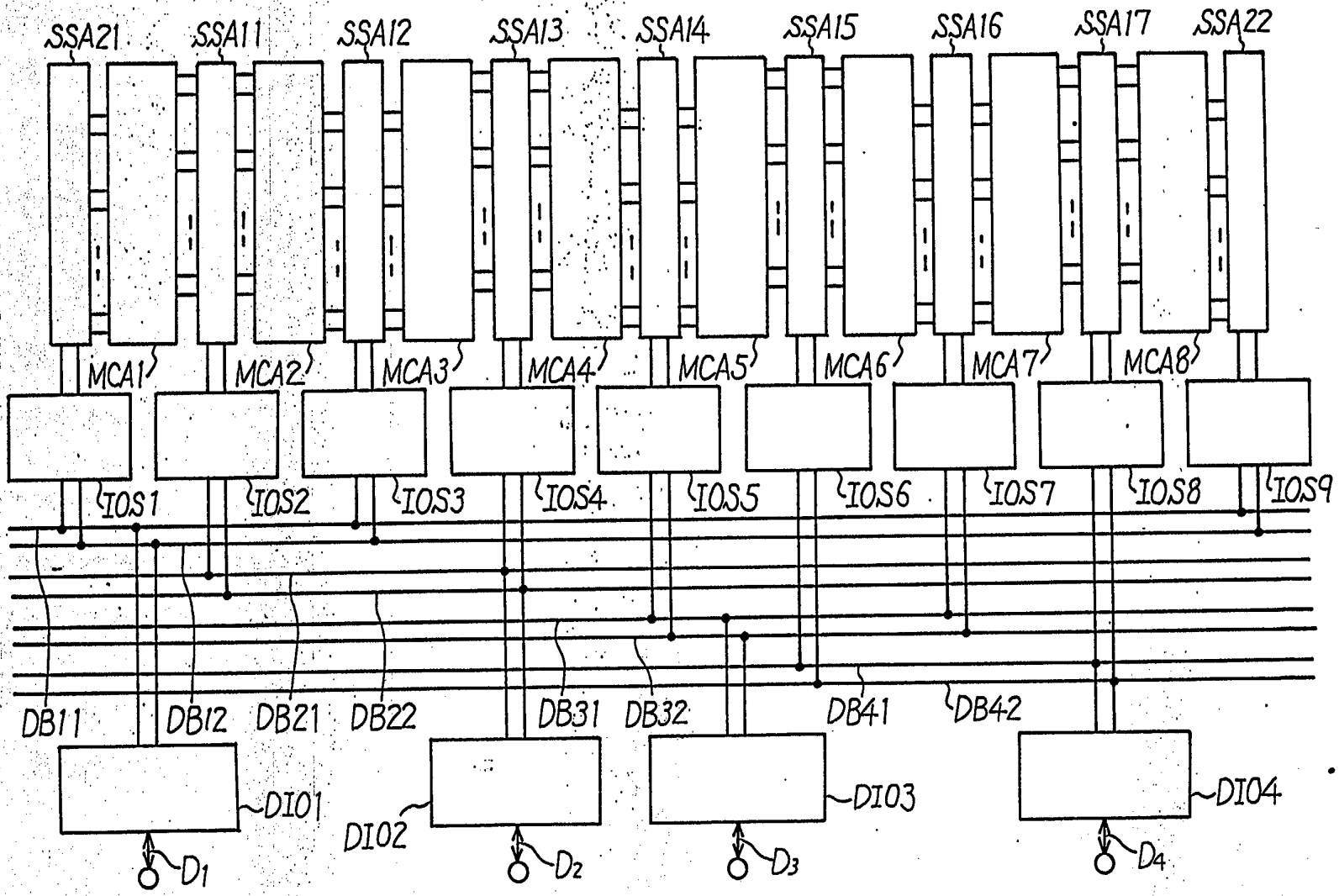
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FIG.3

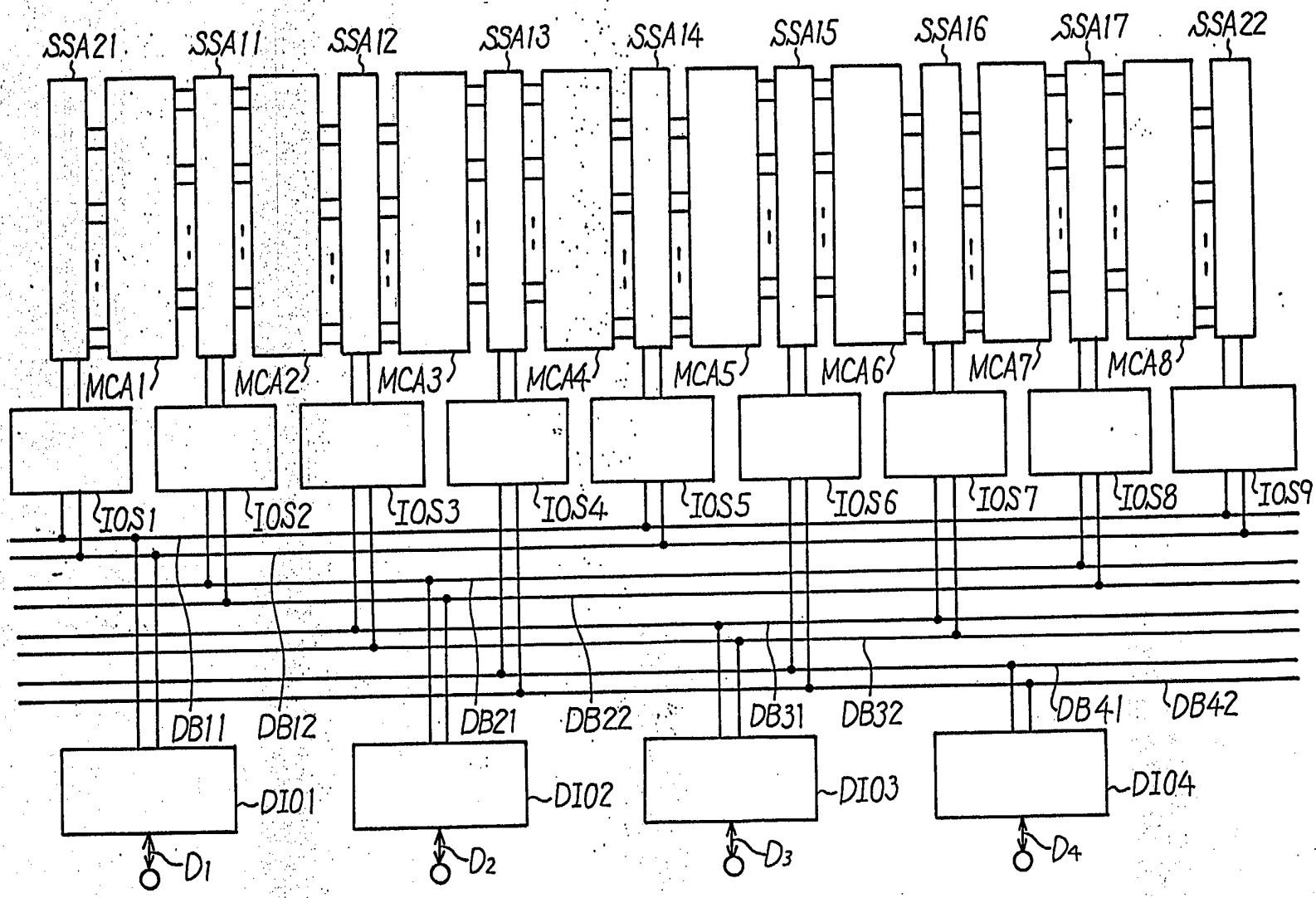
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FIG.4